



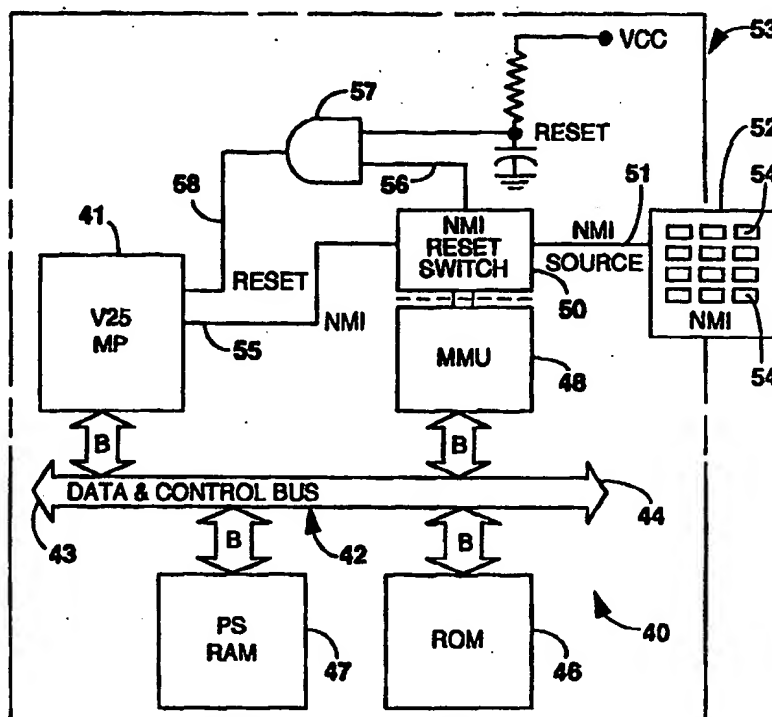
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(54) Title: **SAFE-STOP MODE FOR A MICROPROCESSOR OPERATING IN A PSEUDO-STATIC RANDOM ACCESS MEMORY ENVIRONMENT**

(57) Abstract

A microprocessor circuit (40) including a microprocessor device (41) and a pseudo-static random access memory (47) further includes a switching circuit (50) which is coupled to a non-maskable interrupt (NMI) signal port (55) and to a RESET port (58) of the microprocessor device. The switching circuit intercepts an NMI signal to be applied to the NMI signal port of the microprocessor device and converts an initial NMI signal following a power-down or sleep mode to a RESET signal and applies the RESET signal to the RESET port. NMI signals which occur during normal operation of the microprocessor circuit are routed through the switching circuit directly to the microprocessor device consistent with normal operations. The RESET signal after power-down or sleep mode operations causes the microprocessor device to address ROM (46) until after the pseudo-static RAM has assumed an active, externally refreshed state.



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SAFE-STOP MODE FOR A MICROPROCESSOR OPERATING IN A PSEUDO-STATIC RANDOM ACCESS MEMORY ENVIRONMENT

BACKGROUND OF THE INVENTION

This invention relates generally to microprocessor control systems, and more particularly to microprocessor control systems which include features, such as intermittent power-saving states. Such power-saving features may be of particular advantage in, for example, in microprocessor-controlled equipment which is portable and which is intended to operate on self-contained power sources for extended periods of time.

Certain state-of-the-art portable microprocessor-controlled types of apparatus may operate in conjunction with static memory to retain application programs and operational states during times of shutdown. Retention of operational states may be particularly desirable for portable microprocessor-controlled apparatus. For certain rechargeable battery packs a deep discharge is desired to prevent a loss of power storage capacity. Even if the portable apparatus operates on rechargeable battery packs, it is often considered more convenient from a user standpoint to be able to exchange a battery pack which has exhausted its charge to a fully charged battery pack, rather than to take time to recharge the battery pack which has exhausted its charge.

Static RAM devices, i.e., electronic memory devices which retain their memory cell states without refresh pulses, appear ideally suited to save application programs and microprocessor

1 states during periods of a complete power-down condition of a
2 microprocessor controlled apparatus. A retention of program
3 and microprocessor states on power-down occurrences (for
4 whatever the reason) further permits a user to resume
5 operation after subsequent power-up of a respective
6 microprocessor controlled apparatus, just where the operation
7 had been interrupted by the earlier power-down occurrence.

8 Unfortunately, static RAM devices are often considered,
9 in an overall system perspective, to be comparatively costly
10 and, moreover, the devices are also relatively large in
11 physical size. The physical size of the memory devices in
12 turn affects the physical size of apparatus that houses them.
13 A resultingly relatively large unit is, however, less
14 desirable than a comparatively smaller one, when the units are
15 intended to be handheld, as, for example, portable data
16 collection terminals of an information retrieval system.

17 An alternative to using static RAM devices for saving
18 application programs and microprocessor states during
19 intermittent power-down states, is a use of pseudo-static
20 memory devices which are known as "PSRAM" devices. PSRAM
21 devices require a refresh operation, very much like typical
22 dynamic memory (DRAM) devices often referred to as random
23 access memory or simply as RAM devices. Thus, during normal
24 operation, a memory management unit (MMU) periodically, for
25 example at twelve microsecond intervals, addresses all
26 locations of the memory with refresh pulses. Whenever an
27 apparatus shutdown occurs, a controlling microprocessor (CPU)
28 may cause the MMU to discontinue the application of refresh

1 pulses. When the refresh pulses from the MMU no longer occur
2 at the PSRAM, the PSRAM goes into what is referred to as a
3 "self-refresh" mode. In the self-refresh mode, memory states
4 of or data within the PSRAM are retained by internal refresh
5 operations which require substantially less power than a
6 continuation of refresh operations via the memory management
7 unit (MMU).

8 A serious operational flaw occurs when a microprocessor
9 device (CPU), which requires code access at the top of
10 addressable RAM after a non-maskable interrupt, is sought to
11 be operated in a memory environment consisting entirely of
12 PSRAM devices. PSRAM devices, upon entering a data preserving
13 self-refresh mode or state, become inaccessible to a CPU until
14 they have been restored to a normal operating mode, in which
15 mode the memory devices are refreshed by externally provided
16 refresh pulses, such as by a MMU. In typical power-saving
17 modes of operation, a respective CPU, such as an NEC V25, for
18 example, is placed into a safe-stop state, which permits all
19 operations to be shut down pending receipt of a non-maskable
20 interrupt (NMI). The CPU, on receiving such an NMI "wake-up"
21 signal, seeks to fetch a 4-byte address (referred to as a
22 "vector") from an interrupt vector table (IVT) at the
23 beginning of memory, which in a pseudo-static memory
24 environment would be the PSRAM. Since the PSRAM at that time
25 has not been placed into its normal operational mode, stored
26 data may be lost, and the CPU may not be able to continue its
27 operation.

1 Some computer systems use memory devices other than PSRAM
2 in critical memory locations to be addressed by the
3 microprocessor after shut-down. However, it appears to be
4 desirable, among other reasons for simplicity sake, as well as
5 from a standpoint of design considerations to provide a
6 microprocessor system with intermittent microprocessor
7 shutdown states and with a capability of functioning in a
8 memory environment of PSRAM devices.

9 SUMMARY OF THE INVENTION

10 It is therefore a general object of the invention to
11 provide circuit functions which allow a CPU which has a
12 safe-stop mode to become operational, after a safe-stop
13 shutdown, even though the CPU is operating in a circuit
14 environment which uses pseudo-static RAM (PSRAM) memory.

15 It is yet another object of the invention to provide an
16 interface function for delaying access by a CPU to PSRAM
17 memory until after such PSRAM memory has been restored to
18 normal addressable operation with externally applied refresh
19 signals.

20 It is therefore a further object of the invention to
21 provide a power-saving mode for a CPU or microprocessor which
22 resumes its normal operation from a safe-stop mode on receipt
23 of an NMI signal by addressing PSRAM memory locations.

24 According to the invention, a microprocessor circuit
25 includes a CPU which has a RESET signal port and a
26 non-maskable interrupt (NMI) signal port. The CPU is operable
27 to execute a start-up sequence to a CPU-active state from a
28 ROM memory address in response to receipt of a RESET signal

1 applied to the RESET signal port, and is further operable to
2 resume operation in the CPU-active state RAM upon leaving a
3 power-saving safe-stop state in response to receipt of an NMI
4 interrupt at the NMI signal port. The microprocessor circuit
5 further includes addressable ROM, PSRAM and a memory
6 management unit (MMU). The MMU is communicatively coupled via
7 the data and control bus to the CPU. An NMI-RESET switch
8 circuit arrangement includes a switch for passing an NMI
9 signal which occurs while the CPU is in the CPU-active state
10 to the NMI signal port as a typical operation in the
11 CPU-active state, and which routes an NMI signal occurring
12 while the CPU is in the safe-stop state to the RESET to a
13 signal generator which generates an NMI-generated RESET signal
14 which is applied to the RESET signal port. On receiving the
15 NMI-generated reset signal, the CPU executes a start-up
16 operation from ROM. The start up operation includes a
17 provision for activating PSRAM and for delaying the CPU-active
18 state until after PSRAM has become active.

19 Other features and advantages of the invention will
20 become apparent from reading the detailed description below.

21 BRIEF DESCRIPTION OF THE DRAWINGS

22 The detailed description of the invention may be read in
23 reference to the appended drawing wherein:

24 FIG. 1 is a schematic block diagram representing a
25 microprocessor circuit operable with a sleep mode in a memory
26 environment of static RAM (SRAM) devices;

27 FIG. 2 is a state diagram showing operational states of
28 the microprocessor circuit of FIG. 1;

1 FIG. 3 is a schematic block diagram representing a
2 microprocessor circuit operable with a sleep mode and in a
3 memory environment of pseudo-static RAM (PSRAM) devices in
4 accordance with the invention;

5 FIG. 4 is a schematic diagram of an non-maskable
6 interrupt reset switch (NMI-RESET SWITCH) shown in FIG. 3; and

7 FIG. 5 is a state diagram showing operational states of
8 the microprocessor circuit of FIG. 3, and showing particular
9 operations in accordance with the invention.

10 DETAILED DESCRIPTION OF THE INVENTION

11 Referring to FIG. 1, there is shown a microprocessor
12 circuit which is designated generally by the numeral 10. A
13 controlling circuit element of the microprocessor circuit 10
14 is a microprocessor device 12 which may be placed into a
15 power-saving mode referred to as a sleep mode. As used
16 herein, the term sleep mode refers to a shutdown mode of the
17 microprocessor device 12, as distinguished from a stand-by
18 mode, in which the microprocessor device 12 is not completely
19 shut down, but operates in a slow, power-saving mode. The
20 invention is described in reference to a microprocessor
21 circuit which uses an "NEC V25" as a preferred example for
22 implementing features of the invention. It is to be
23 understood that other microprocessor devices may be used in
24 implementing features of the invention and in achieving the
25 advantages referred to herein. However, the V25
26 microprocessor device 12 depicted schematically in FIG. 1 has
27 been found to satisfy adequately the requirements of
28 implementing the invention as described herein.

1 In reference to both FIGS. 1 and 2, FIG. 2 relates to
2 operations of the microprocessor device 12 of FIG. 1, wherein
3 the microprocessor obtains operational data either from
4 permanent memory, such as read-only memory 14 (ROM), or from
5 static memory 15 (Static RAM). Both the ROM 14 and the Static
6 RAM 15 are coupled in a known and typical manner to respective
7 data and control ports of the microprocessor device 12 via a
8 typical data and control bus 16, as shown by the "data and
9 Control BUS" arrow and its coupling extensions labelled "B".
10 Open arrowheads 17 and 18 identify the bus 16 as extending
11 typically to further input-output ports and related
12 microprocessor circuit elements or functional devices, such as
13 disk drives or communications circuits coupled to respective
14 ports. The use of these devices or circuits, also referred to
15 as peripherals, is well known in the art, but their selection
16 is usually one of choice. Thus, the presence of selected
17 peripherals is schematically shown by the respective arrows 17
18 and 18.

19 The microprocessor device 12 operates in a controlled
20 sequence of operations as dictated by a control program found
21 by selectively accessing memory locations of the ROM 14 and
22 the Static RAM 15. The state of operations (or temporary wait
23 periods) may be interrupted by signals appropriately referred
24 to as "interrupts" or interrupt signals. An interrupt signal
25 which requires action by the microprocessor device 12 is known
26 as a "non-maskable interrupt" signal or "NMI" signal. An NMI
27 signal alerts the microprocessor device 12 to a) check for
28 what type of interrupt signal has been received, and b) to

1 perform an operation or to respond as prescribed by the
2 control program when the presence of the particular type of
3 interrupt signal has been indicated.

4 Two types of operations by the microprocessor device 12
5 are of interest in describing the invention. A first type of
6 operation is a standard POWER-ON RESET. A power-on reset
7 occurs typically on each start-up, typically a "cold start",
8 when the power is first applied to the microprocessor circuit
9 10. All circuit devices or functional units coupled to and
10 forming an integral part of the microprocessor circuit 10 are
11 generally reset when power is first applied to them. This may
12 be true, even though it may be desirable to then reload saved
13 application program parameters into memory or other elements,
14 so as to continue with an operation at a point at which the
15 operation was interrupted prior to the most recent shut-down.
16 To assure a "clean start", the power-on reset applied to the
17 microprocessor device 12 is a logical "low" signal which is
18 sustained for a period of "substantial" length following the
19 application of power to the microprocessor circuit 10 to allow
20 all circuit elements to be ready for operation before the
21 clock signal triggers the microprocessor into action. Thus,
22 system voltage (VCC) is applied to a reset port 21 of the
23 microprocessor device 12 via an RC delay circuit 21 which has
24 a time constant to generate, in the preferred example, a delay
25 of 100 milliseconds. During the initial "power-on reset"
26 period the receipt of an non-maskable interrupt (NMI) signal
27 is undesirable and might interfere with the proper reset
28 operation. Consequently, an NMI signal input line 23 to an

1 NMI port 24 of the microprocessor device 12 is AND-gated at an
2 AND-gate 25 with an NMI holdoff RC delay circuit 26. The time
3 constant of the RC delay circuit 26 is chosen to generate on
4 start-up a time delay which blocks NMI signals for a time
5 period following power-up of the circuit 10, causing an output
6 of the AND-gate 25 (via signal line 27) to remain low during
7 the period of the delay. In a preferred embodiment, the
8 duration of the NMI holdoff is chosen to be 500 milliseconds,
9 for example.

10 In a normal start-up of the microprocessor 10, to arrive
11 at running an applications program, as shown by the "RUN
12 PROGRAM" state 30 in FIG. 2, the microprocessor circuit 10
13 either follows a path via an "OFF" state 31 and a "POWER ON
14 RESET" state 32, or from a "SAFE STOP" state 33 via a "WAKE-UP
15 NMI" state 34. Except for an initial operation of the
16 microprocessor circuit 10, a start-up via the "POWER ON RESET"
17 state also originates from the "SAFE STOP" state 33. A
18 difference in the start-up procedure is that on a reset, the
19 microprocessor 12 accesses the ROM memory locations 14, while
20 on resuming operation after a WAKE-UP NMI, the microprocessor
21 12 jumps to an interrupt vector table which would typically be
22 located at the lowest memory locations of the Static RAM
23 memory 15.

24 While running a program, i.e., while being in the normal
25 operational state 30, the microprocessor circuit 10 may be
26 programmed to time out after a set time interval of
27 non-interventive activity by an operator, for example after a
28 period of one minute during which the microprocessor 12 has

1 not received a keyboard entry NMI. A resulting time-out path
2 to the "SAFE STOP" state 33 is shown by a direct path 35.
3 Another path to the "SAFE STOP" state 33 is shown via a
4 "SHUT-DOWN NMI" state 36. If the time-out timer for
5 initiating a safe stop, or sleep mode, in the microprocessor
6 12 initiates a time-out NMI, the time out path 35 may be
7 considered to be identical with the path via the "SHUT-DOWN
8 NMI" state 36. A typical shut-down NMI, other than the
9 time-out NMI, may be caused, for example, by a "low battery"
10 indication. Another reason for the microprocessor 12
11 receiving a shut-down NMI may be because of a sudden impending
12 power loss, other than one caused by a steadily discharging
13 battery. An indication of such a sudden power loss to the
14 microprocessor circuit 10 may originate, for example, from a
15 hardware safety switch coupled to a power pack compartment or
16 connection. In all instances of receiving a time-out or
17 shut-down NMI, the microprocessor circuit 10 would be
18 instructed to stop operating in any applications program and
19 immediately store all, then current, operating parameters in,
20 for example, separately battery-backed memory, or other
21 non-volatile memory for future recall. Any start-up after
22 reaching the "SAFE STOP" state 33 be it via the "POWER ON
23 RESET" or via the "WAKE-UP NMI" permits a user to restore the
24 most recent state of operation of the microprocessor circuit,
25 thus, resume operations where they had been left off prior to
26 the microprocessor 12 entering the sleep mode. Use of the
27 above-described power-saving sleep mode operation presupposes
28 the presence of non-volatile memory for storing all necessary

1 operating parameters while the microprocessor is in the sleep
2 mode. Moreover, it presupposes ready accessibility of such
3 non-volatile memory to recall the operating parameters when
4 resumption of operations by the microprocessor 12 is called
5 for.

6 Since pseudo-static RAM memory requires to be
7 re-activated from its self-refresh mode before it may and can
8 be accessed by a microprocessor to retrieve or store data, the
9 use of pseudo-static RAM memory in place of the Static RAM
10 memory 15 as described with respect to FIG. 1 has been found
11 to present operational problems. FIG. 3 shows a schematic
12 diagram of a control circuit 40, and particularly a
13 microprocessor circuit 40, which overcomes such operational
14 problems. The microprocessor circuit 40 includes a control
15 device, particularly a microprocessor device 41 ("V25 MP")
16 which operates by accessing and communicating with memory
17 locations and input/output devices via a communications and
18 address bus 42, as schematically represented by arrows
19 identified as "DATA & CONTROL BUS" and their respective
20 extensions identified as "B". Electrical connections via a
21 plurality of data and control lines generally communicatively
22 couple selected devices by device addresses or control
23 signals. Specific data signals may be communicated between,
24 for example, the microprocessor device 40 and another selected
25 device via the data and control bus 42. The placed address
26 signal uniquely identifies a particular device or a memory
27 location to which the corresponding data signal may be
28 written, or from which data signals such as one or more data

1 bytes may be fetched. Additional I/O capabilities to couple
2 any of a number of available devices to the data and control
3 bus 42 are schematically indicated by the open arrows heads 43
4 and 44 of the bus 42. Memory locations wherein a control
5 program or BIOS code is stored, may be a typical masked, i.e.
6 permanent, read only memory, or an electrically changeable
7 FLASH read-only memory, shown as "ROM" memory 46.
8 Read-and-write memory accessed by the microprocessor device 41
9 during normal operations for storing or retrieving data may be
10 comprised of, in accordance with the present invention,
11 entirely of pseudo-static RAM, shown as "PS RAM" memory 47.
12 The term "pseudo-static memory" as used herein is that type of
13 electronic memory which has a normal or active operating mode
14 during which the memory cells of the memory 47 are
15 periodically refreshed by refresh pulses applied from an
16 external pulsing source. During the active mode the memory is
17 addressable and accessible to write data into and retrieve
18 data from respectively addressed memory cells. External
19 refresh pulses, which are required during an active state of
20 the pseudo-static RAM memory 47, are generated in the
21 preferred embodiment by the microprocessor device 41 (V25 MP).
22 The refresh pulses are routed to the pseudo-static memory 47
23 via a memory management unit "MMU" 48, such as via the data
24 and control bus 42. It should be understood that the data and
25 control bus 42 represents typical address and pulse
26 connections which are coupled to respective address and signal
27 ports on individual devices of the pseudo-static memory 47.
28 In general, an external refresh operation for the

1 pseudo-static memory 47 may be provided by a circuit or
2 network including a refresh pulse generator and a refresh
3 pulse distributor. The refresh pulse network would be coupled
4 to the memory 47 to address and distribute refresh pulses to
5 individual memory cells of the memory 47 in predetermined
6 refresh intervals. The periodically applied refresh pulses
7 are required to maintain the pseudo-static memory 47
8 externally refreshed and active. The combination of the
9 microprocessor circuit 41, the coupling network of the data
10 and control bus 42, and the memory management unit 48 could,
11 for example, be a single integrated circuit coupled to
12 respective refresh ports of the memory 47. In another
13 embodiment, a refresh pulse generator may be a circuit
14 separate from the microprocessor device 41, and the
15 microprocessor device 41 as a control device may control the
16 refresh pulse distributor or memory management unit 48.
17 According to the preferred and described embodiment, the
18 memory management unit 48 distributes the refresh pulses to
19 the pseudo-static RAM memory 47 to maintain the memory 47
20 active. During an inactive state, whenever the external
21 refresh pulses are not applied to the pseudo-static RAM memory
22 47, the memory 47 enters a self-refresh mode. In the
23 self-refresh mode, the power consumption of the pseudo-static
24 RAM memory 47 is at a minimum and the presence of normal
25 system power is not required. However, in such self-refresh
26 mode, the pseudo-static RAM memory 47 is not accessible for
27 storing or retrieving information, as, for example, by the
28 microprocessor device 41 during routine operations.

1 Therefore, on any start-up, whether from a power-saving sleep
2 mode, or from an OFF condition in which battery power was
3 either removed or disconnected, the pseudo-static RAM memory
4 47 needs to be restored to an active, externally refreshed,
5 condition before it can be addressed by the microprocessor
6 device 41.

7 On Reset, the microprocessor device 41 obtains initial
8 operating instructions from masked memory (ROM) 46. However,
9 a typical wake-up NMI would cause the microprocessor device 41
10 to seek access to the pseudo-static memory 47 before the
11 memory 47 might be restored to its active state. The
12 microprocessor circuit 40 includes advantageously an NMI
13 switch ("NMI RESET SWITCH") 50 or switching circuit 50. The
14 switching circuit 50 is controllable to distinguish between
15 NMI signals which are applied after an interruption of power
16 to the microprocessor circuit 40, and those NMI signals which
17 occur in the course of normal operation of the microprocessor
18 circuit 40. As may have become adequately apparent from the
19 above discussion, prior power interruptions, i.e., those which
20 have caused the pseudo-static memory 47 to go into its
21 self-refresh mode, require a significant delay to be imposed
22 on commencement of operation by the microprocessor device 41,
23 such as the delay generated by the described reset operation.
24 A "POWER-ON RESET" provides for the pseudo-static memory 47 to
25 become activated before the microprocessor device 41 seeks
26 access to the memory 47.

27 On first glance a simple solution appears to be to route
28 all NMI signals through a "POWER ON RESET" as described above

1 in reference to FIG. 2. Closer examination reveals that to
2 use the reset delay route also requires that the
3 microprocessor circuit first be placed into a "SAFE STOP"
4 state as described above. Such cumbersome and time consuming
5 operation would be less than desirable if made applicable to
6 all NMI signals during normal microprocessor operations. The
7 routing of all NMI signals through actual or simulated device
8 reset operations may, however, be circumvented by the
9 intervening function of the switching circuit or NMI switch
10 50.

11 The NMI switch 50 receives an NMI signal via an "NMI
12 SOURCE" port or connection 51. The NMI signal may have
13 originated at any NMI source, hence any device capable of
14 sending an NMI signal, a schematically drawn keyboard 52
15 representing generically any and all such NMI sources. Using
16 the keyboard 52 as an example of an NMI source for itself, the
17 keyboard 52 may be a keyboard of a portable data device, such
18 as a hand-held data collection terminal 53, represented
19 schematically by the box 53 drawn in phantom lines and
20 enclosing the microprocessor circuit 40. A depression of any
21 key 54 of the keyboard 52 would cause an NMI signal to be sent
22 to the microprocessor device 41. As shown in FIG. 3, the NMI
23 switch 50 intercepts all NMI signal and changes the operation
24 of the microprocessor circuit 40 by converting all power-up
25 related NMI signals to power-up reset signals, while passing
26 all other NMI signals via an NMI port or connection 55
27 directly to the microprocessor device 41. The switch 50
28 converts, for example, a "wake-up" NMI in a pulse-shaping

1 operation to a reset signal while inhibiting the application
2 of the NMI signal to the microprocessor circuit 41. The reset
3 signal generated by the NMI switch 50 is a logical low signal
4 which is sustained for the prescribed reset period. The
5 generated reset signal becomes gated via an input port 56 of
6 an AND-gate 57 to a reset port 58 of the microprocessor device
7 41.

8 FIG. 4 is a schematic representation of functional
9 elements of the NMI switch 50. It should be understood that
10 the NMI switch 50 may, in a preferred embodiment, be
11 physically integrated on the silicon chip of the memory
12 management unit 48 (see FIG. 3), though the NMI switch 50 may
13 be separate, at least functionally, as indicated by the
14 interface dotted line, also shown in FIG. 3. In a preferred
15 embodiment, the NMI switch 50 receives device select and data
16 input signals via the data and control bus 42 or directly from
17 the memory management unit 48. Further in reference to FIG.
18 4, input signals shown on the left-hand side of the NMI switch
19 50 are the NMI signal source port 51, a data bit source or a
20 data port 61 ("DATA BIT 0"), and a device select ("ADDRESS
21 SELECT") bus connection 62.

22 In reference to FIGS. 3 and 4, a data bit at the data
23 port 61 is read either into data port "D1" or into data port
24 "D2" of respective data latches 66 or 67 (DATA LATCH1 or DATA
25 LATCH2), depending on the address select signal appearing at
26 the ADDRESS SELECT bus connection 62. The data latch 67
27 functions as a switch 67 to either block or unblock an NMI
28 signal appearing at the NMI source port 51 from being applied

1 to the microprocessor device 41. The data latch 66 is an NMI
2 routing switch which directs an NMI signal (other than one
3 blocked by the operation of the data latch 67) to be applied
4 either as a reset signal to the reset port 58, or as an NMI
5 signal to the NMI port 55 of the microprocessor device 41.

6 Tracing the signals through the switch 50, an NMI signal,
7 as an edge triggering signal is applied via the NMI port 51
8 through a first OR-gate 68 to one of the input ports of a
9 second, NMI signal OR-gate 71 and a third, RESET OR-gate 72,
10 respectively. A Q1 data output from the data latch 66
11 constitutes the other, second OR-gated input to the OR-gate
12 71. A data output from the output node Q2 of the second data
13 latch 67 is applied as a second OR-gated signal to the OR-gate
14 68 and thus, as an output OR-gated with an NMI source signal
15 to the OR gates 71 and 72. An inverted data output "not-Q1"
16 of the data latch 66 is applied as a second OR-gated input of
17 the third OR-gate 72. An active low output node 73 from the
18 OR-gate 71 constitutes an NMI signal which appears at the NMI
19 signal line 55 which is also the NMI signal port 55 of the
20 microprocessor device 41 (see FIG. 3). An output node 74 from
21 the OR-gate 72 is applied through a "ONE SHOT" function device
22 75 to the input port 56 of the AND-gate 57 (see FIG. 3). The
23 ONE SHOT device 75 is a typical pulse-shaping device for
24 converting, in this particular application, an active signal
25 edge to a low RESET signal pulse which is sustained for the
26 desired reset time period of 100 milliseconds, as an example.
27 In general, the conversion of the active edge-triggered signal
28 to a required pulse of a desired sustained length may be

1 adapted to suit the reset needs of the particular
2 microprocessor device 41.

3 Referring now to FIGS. 3 and 5, the use of the
4 intervening NMI switch 50 described in reference to FIGS. 3
5 and 4, alters start-up procedures of the microprocessor device
6 41 with respect to the start-up operations of the
7 microprocessor device 12 described with respect to FIGS. 1 and
8 2. According to the state diagram of FIG. 5, an active
9 operating state includes processing of NMI signals in a
10 routine operating manner. Also, if a shut-down NMI signal is
11 received, as shown by the transition state 81 ("SHUT-DOWN
12 NMI"), the microprocessor circuit is placed into a safe stop
13 mode 82 ("SAFE STOP"), regardless of whether a the ensuing
14 state is a total shut-down of the portable data collection
15 terminal 53, or whether the shut-down mode is a contemplated
16 power saving temporary sleep mode. Once in the safe stop
17 state 82, a start-up from the sleep mode generates a wake-up
18 reset state 83 ("WAKE-UP RESET"), according to which a the
19 wake-up NMI signal is intercepted by the NMI switch 50 and is
20 converted to a reset signal, as described, which is applied
21 via the AND-gate 57 to the reset port 58 of the microprocessor
22 circuit 41, as if a reset signal had been generated in
23 response to an initial start-up 84 ("POWER-ON RESET"), after
24 a power-off state 85 ("OFF"). In either route, in response to
25 a wake-up NMI or from a complete off state, the microprocessor
26 circuit 40 obtains initial instructions from the ROM memory
27 46. Addressing the pseudo-static memory 47 is delayed for a
28 period sufficient to return the pseudo-static memory 47 to the

1 external refresh mode through refresh signals generated by the
2 microprocessor and applied by the memory management unit 48.
3 The corresponding memory start-up delay is shown in FIG. 5 by
4 a wait state 88 ("WAIT FOR PSRAM"). Both the power-on reset
5 84 and the wake-up reset 83 invariably places the
6 microprocessor device 41 into the wait state 88 for the
7 duration of the reset time period.

8 The operation of the NMI switch 50, consequently, allows
9 the microprocessor circuit 40 to operate with a full
10 complement of pseudo-static memory 47 in an operational mode
11 wherein all NMI signal operation received while the
12 pseudo-static memory 47 is active are executed in a normal
13 interrupt mode. On the other hand, any time an NMI is
14 received while the pseudo-static memory is in a self-refresh
15 mode, a delay is generated by converting the NMI signal to a
16 reset signal to allow the pseudo-static memory to be in an
17 active state at the time when the microprocessor device 41
18 first resumes operation. An apparent indistinction between
19 the "POWER-ON RESET" condition 84 and the "WAKE-UP RESET"
20 condition or state 83 may be clarified, if so desired, by a
21 data latch which latches, for example, a logical "1" signal to
22 remain high under all conditions except when power is lost to
23 the portable data collection terminal 53. In the preferred
24 embodiment, the microprocessor device 41, which is an NEC V25
25 device, provides internally a data bit location referred to as
26 standby control bit (STBC) which fulfills the desired
27 condition. Thus, after any reset, ROM instructions may be
28 used to query the "STBC" register of the microprocessor device

1 41 to determine whether the reset occurred because of an
2 initial power-up operation or because of a power interruption,
3 caused, for example, by replacing a low battery of the
4 portable data collection terminal 53. The data collection
5 terminal 53 may, in the latter case, display an informational
6 message to an operator to query, for example, whether an
7 application program is to resume at a prior point of
8 interruption or whether the unit is to be otherwise
9 initialized. Thus, after a power interruption to the
10 hand-held data collection terminal 53, the software
11 instructions contained within the ROM memory 46 shown in FIG.
12 3 may, after causing a display of an appropriate prompt to an
13 operator, may cause a logical "1" to be written to the STBC
14 bit address of the microprocessor device 41.

15 Though certain variations and modifications have already
16 be referred to or described, it is understood various other
17 changes and modifications in the use and implementation of the
18 described embodiments are possible without departing from the
19 spirit and scope of the invention as set forth in the claims.

WHAT IS CLAIMED IS:

1 1. Apparatus for controlling access to pseudo-static memory
2 within which pseudo-static memory data may be stored and from which
3 such stored data may be retrieved during active periods of the
4 pseudo-static memory, the pseudo-static memory remaining
5 addressable and active during periods of externally applied refresh
6 pulses and becoming self-refreshing and non-responsive during
7 periods without externally applied refresh pulses, the apparatus
8 comprising:

9 a refresh pulse network including a refresh pulse generator
10 and a refresh pulse distributor connectable to pseudo-static memory
11 and including means for applying refresh pulses to such
12 pseudo-static memory to maintain such memory in an active and
13 addressable state;

14 a control device communicatively connectable to the
15 pseudo-static memory to access the pseudo-static memory in response
16 to receipt of a non-maskable interrupt signal from one of a
17 plurality of NMI sources, and coupled to the refresh pulse
18 distributor to inhibit the refresh pulse distributor from applying
19 refresh pulses from the refresh pulse generator to the
20 pseudo-static memory during an address-inactive state of the
21 pseudo-static memory; and

22 a switching circuit coupled between the control device and the
23 NMI source to intercept a non-maskable interrupt signal to the
24 control device, the switching circuit including a non-maskable
25 interrupt signal routing switch having a first switched output node

26 coupled to an NMI port and having a second node, a pulse-shaping
27 circuit having an input lead coupled to the second node of said
28 routing switch and having an output node coupled to a reset port of
29 the control device, the switching circuit being operative whenever
30 the pseudo-static memory is in an address-inactive state to convert
31 an initial non-maskable interrupt signal occurring at the
32 conclusion of an address-inactive state of the pseudo-static memory
33 to a reset pulse, the reset pulse being routed to the reset port
34 and inhibiting access of the control device during a period within
35 which the pseudo-static memory remains in the address-inactive
36 state.

1 2. Apparatus according to claim 1, wherein the control
2 device is a microprocessor device.

1 3. Apparatus according to claim 1, wherein the control
2 device is a microprocessor device, wherein the refresh pulse
3 generator of the refresh pulse network is included within the
4 microprocessor device, and wherein the refresh pulse distributor of
5 the refresh pulse network is a memory management unit coupled to
6 the refresh pulse generator of the microprocessor device.

1 4. Apparatus according to claim 3, further comprising a data
2 and control bus, and wherein the memory management unit, the data
3 and control bus, the microprocessor device and the switching
4 circuit are comprised within a control circuit of a portable data
5 collection terminal.

1 5. Apparatus according to claim 4, wherein the plurality of
2 NMI sources includes a keyboard of the portable data collection
3 terminal.

FIG. 1

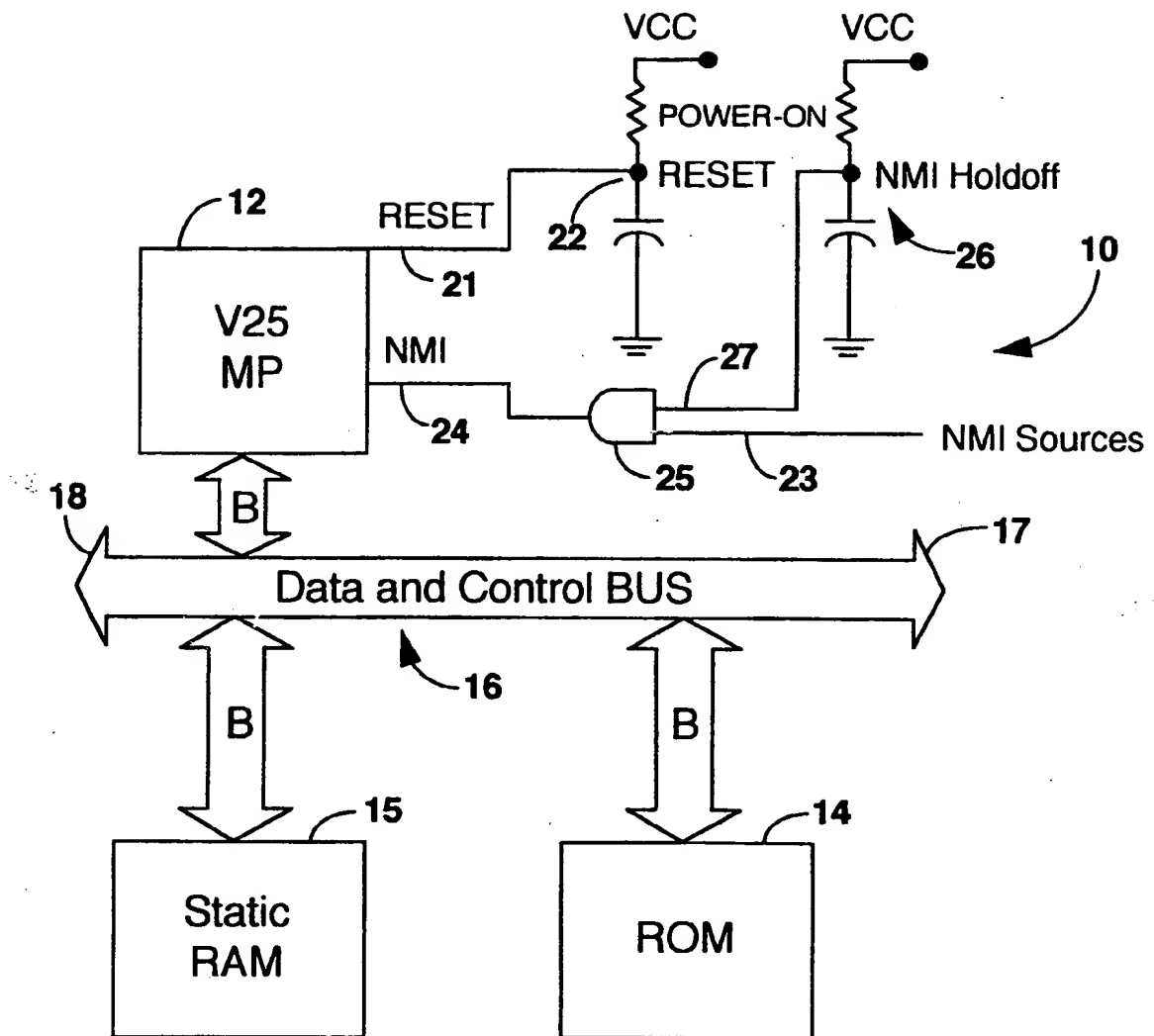


FIG. 2

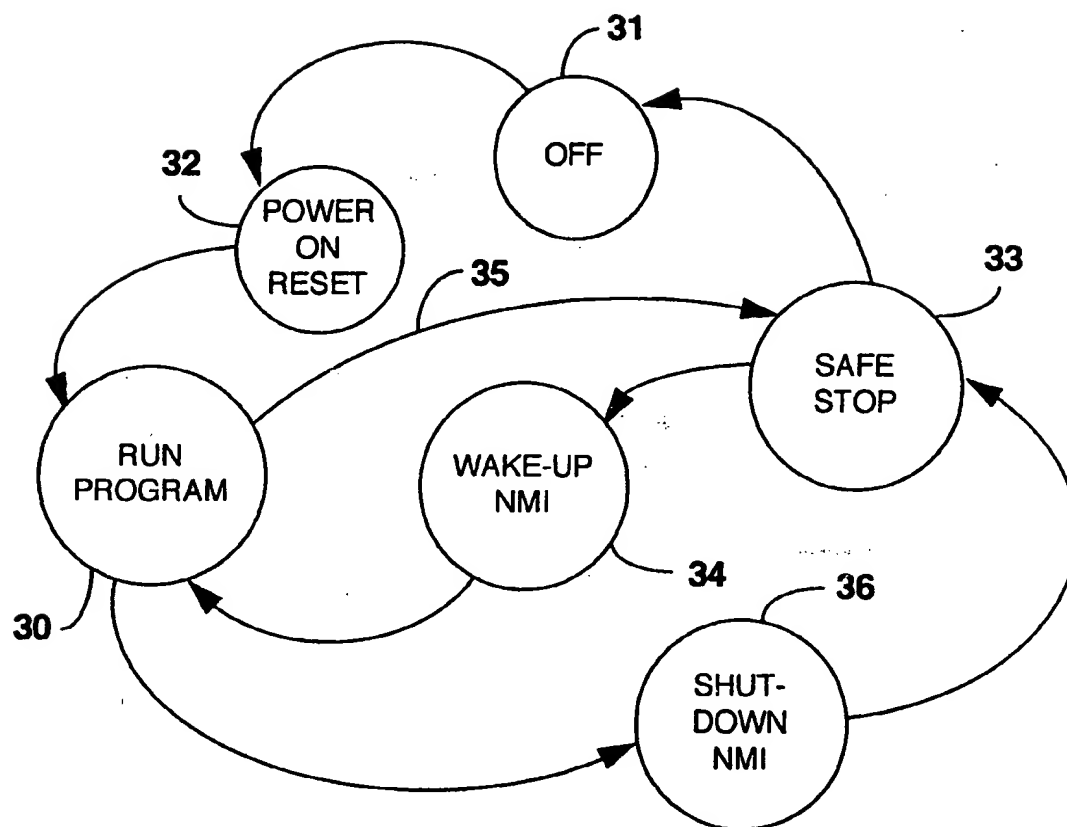


FIG. 3

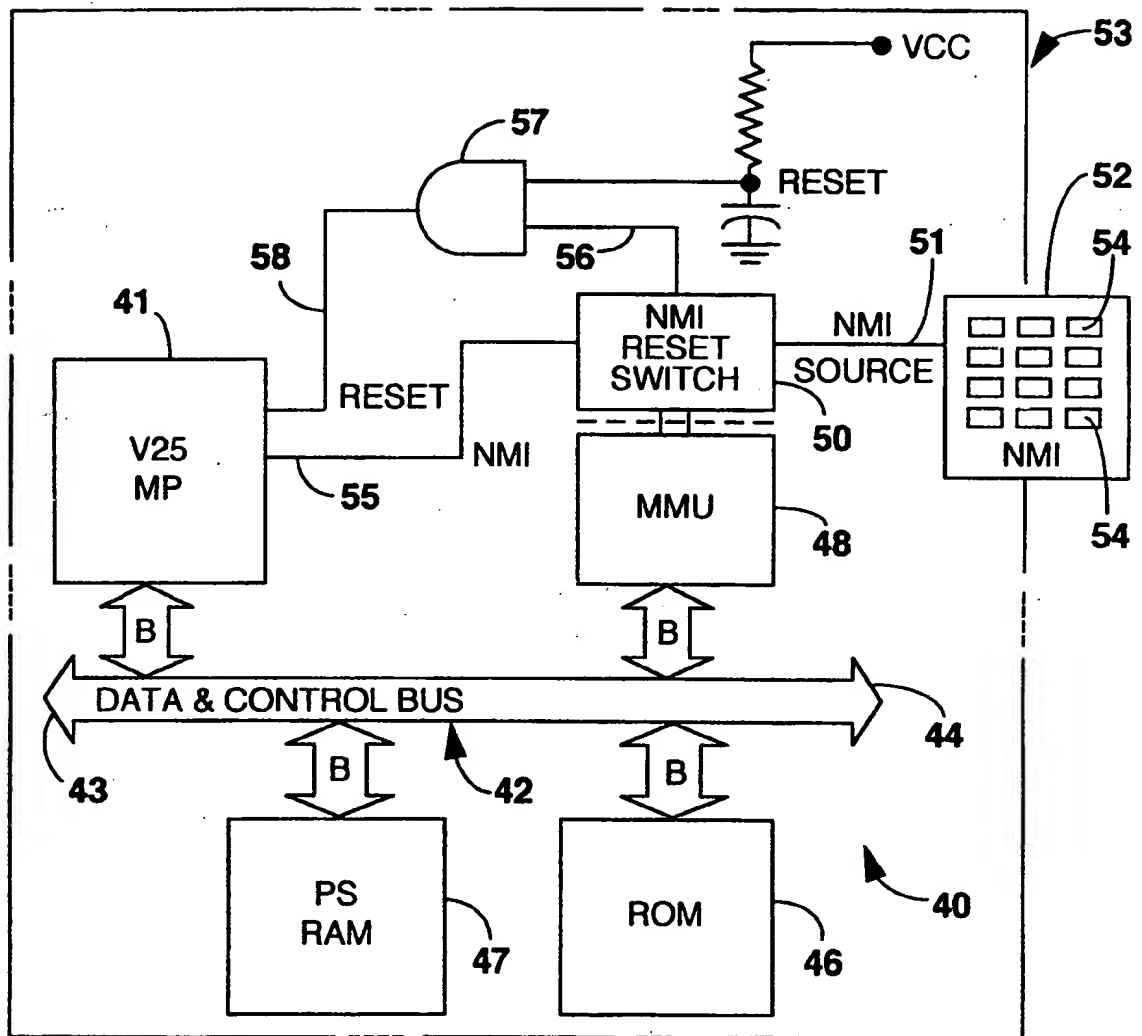


FIG. 4

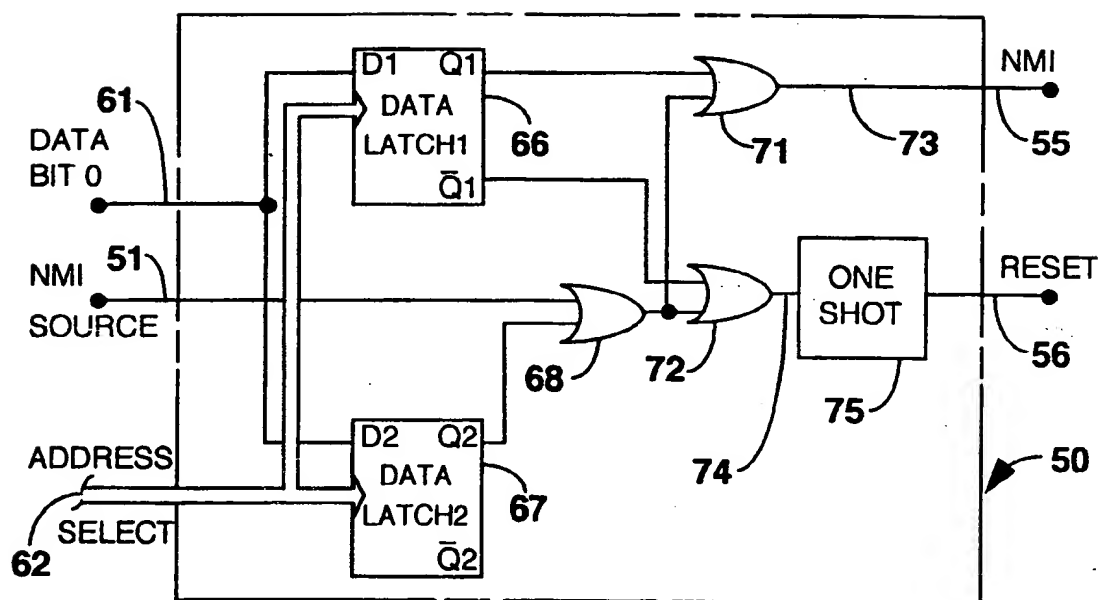
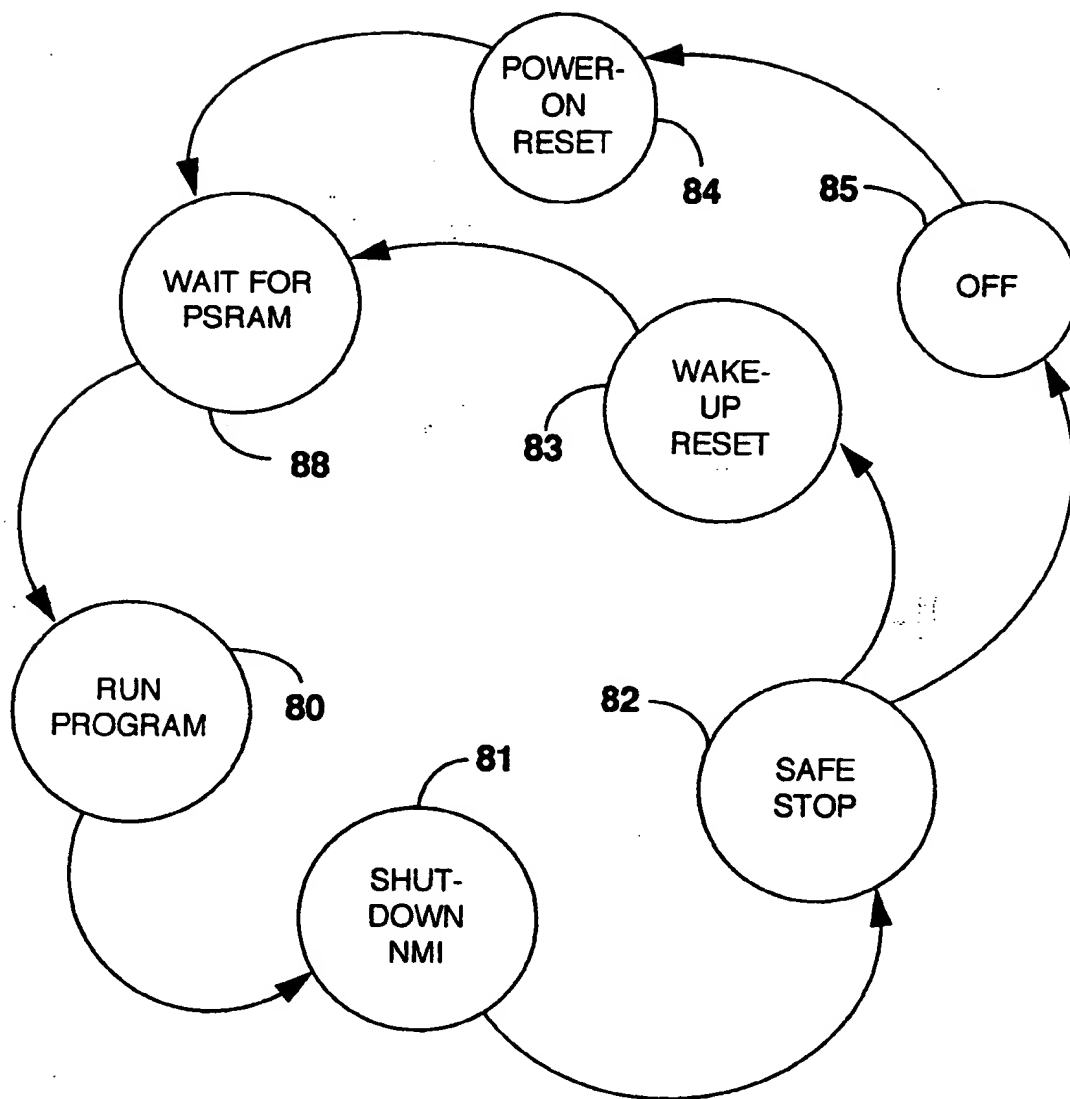


FIG. 5



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US95/00220

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 1/24, 1/32, 12/00; G11C 11/406

US CL :395/425, 725, 750;365/222, 227, 228, 229

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/425, 725, 750;365/222, 227, 228, 229

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, DIALOG

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,229,970 (LEE ET AL) 20 July 1993, col. 1-3.	1-5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	* T	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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* E		
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* Y		document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
* Z		document member of the same patent family

Date of the actual completion of the international search

09 MARCH 1995

Date of mailing of the international search report

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